CLAIMS

1. An article of manufacture comprising:

a machine-readable medium having a plurality of machine readable instructions, wherein when the instructions are executed by a processor, the instructions provide to manage a system for:

dividing a flash memory block into individual data areas or sectors, wherein each sector has an associated header for identifying a sector's status; and

rearranging a plurality of Power Loss Recovery (PLR) status bits such that all the PLR status bits are extracted from a header and data area and coalesced into a predetermined region.

2. The article of manufacture of claim 1 wherein the system is a flash media.

3. The article of manufacture of claim 2 wherein the flash media comprises a flash memory to support error correcting code (ECC).

4. The article of manufacture of claim 3 wherein the flash memory supports multilevel states.

5. The article of manufacture of claim 1 wherein the predetermined region does not have ECC protection and relies on level 1 and level 4 states.

6. A method for organizing PLR status bits comprising;

storing a plurality of PLR status bits in a predetermined region within a flash memory; and

selecting a multi-level state for the plurality of PLR status bits.

7. The method of claim 6 further comprises ECC protection for the flash memory except for the PLR status bits.

8. The method of claim 6 wherein selecting one of a plurality of multi-state levels comprises selecting either a level 1 or level 4 states for the plurality of PLR status bits.

9. The method of claim 6 wherein the flash memory is incorporated within a flash media system.

10. A method for organizing PLR status bits comprising;

storing a plurality of PLR status bits in a predetermined region within a flash memory;

selecting a multi-level state for the plurality of PLR status bits; and

protecting the flash memory with ECC except for the PLR status bits.

11. The method of claim 10 wherein selecting one of a plurality of multi-state levels comprises selecting either a level 1 or level 4 states for the plurality of PLR status bits.

12. The method of claim 10 wherein the flash memory is incorporated within a flash media system.

13. An article of manufacture comprising:

a machine-readable medium having a plurality of machine readable instructions, wherein when the instructions are executed by a processor, the instructions provide to manage a system for:

rearranging a plurality of Power Loss Recovery (PLR) status bits such that all the PLR status bits are extracted from a header and data area and coalesced into a predetermined region;

selecting a multi-level state for the plurality of PLR status bits; and

protecting the flash memory with ECC except for the PLR status bits.

14. The article of manufacture of claim 13 wherein the system is a flash media.

15. The article of manufacture of claim 14 wherein the flash media comprises a flash memory to support error correcting code (ECC).

16. The article of manufacture of claim 13 wherein the predetermined region does not have ECC protection and relies on level 1 and level 4 states.

17. A flash memory to support ECC comprising:

a flash memory block divided into individual data areas and sectors, wherein each sector has an associated header for identifying a sector's status; and

a plurality of Power Loss Recovery (PLR) status bits such that all the PLR status bits are extracted from a header and data area and coalesced into a predetermined region;

the ECC to detect and correct errors for the flash memory block except for the PLR status bits.

18. The apparatus of claim 17 wherein the flash memory supports multi-level states.

19. The apparatus of claim 18 wherein PLR status bits are Level 1 or Level 4 states.

20. A system comprising:

a first logic to request data from a flash memory, wherein the flash memory comprises:

individual data areas and sectors, wherein each sector has an associated header for identifying a sector's status;

a plurality of Power Loss Recovery (PLR) status bits such that all the PLR status bits are extracted from a header and data area and coalesced into a predetermined region; and

the ECC to detect and correct errors for the flash memory block except for the PLR status bits.

21. The system of claim 20 further comprising a wireless interface.

22. The system of claim 20 wherein the flash memory supports multi-level states.

23. The system of claim 20 wherein PLR status bits are Level 1 or Level 4 states.

24. The system of claim 20 wherein the first logic is a microprocessor.

25. The system of claim 20 further comprising a second logic to request data from the flash memory, the second logic is a digital signal processor.